Electronic Version
Stylesheet Version v1.1.1

Description

[LOW TEMPERATURE POLYSILICON THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING THE SAME]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92108769, filed April 16, 2003.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a low temperature polysilicon (LTPS) thin film transistor (TFT) and method of manufacturing the same. More particularly, the present invention relates to a highly flexible manufacturing of fabricating low temperature polysilicon thin film transistors.

[0004] Description of Related Art

[0005] An outcome of the rapid progress in high-tech products is the popularity of video products such as digital video or

imaging devices in our daily life. To be useful, these digital video and imaging devices must provide a high-quality display so that a user can operate a controlling device after reading some important information disseminated from the display.

[0006] Thin film transistors are the principle driving devices inside a liquid crystal display (LCD). With a flat and streamline design, LCD has become one of the most popular vertically erected desktop monitors serving personal computers and game machines. Among the thin film transistor liquid crystal displays, one type of display has internal thin film transistors fabricated using a polysilicon technique that can reduce electron mobility relative to a thin film transistor fabricated using the conventional amorphous silicon technique. In general, a thin film transistor having higher electron mobility can have a smaller dimension and a larger aperture ratio so that the display is able to attain a higher brightness level and consume less power. Furthermore, the increase in electron mobility also permits the fabrication of part of the driving circuits and the thin film transistors together on a glass substrate to improve the performance and reliability of the liquid crystal display panel. Therefore, overall cost of producing the

liquid crystal display panel is lowered considerably compared with the amorphous silicon thin film transistor liquid crystal display. In addition, since the polysilicon can be fabricated into light and thin sheets of material, it finds many applications in lightweight and low-power portable equipment. However, the conventional method of annealing the amorphous silicon to transform the amorphous silicon into polysilicon demands a temperature of over 600°C. Hence, the substrate must be fabricated using heat-resistant quartz material. Yet, a quartz substrate not only is more expensive than a glass substrate, but a quartz substrate having a linear dimension greater than 2 to 3 inches is also difficult to produce. Because of such limitations, polysilicon thin film transistor panels are formed in relatively small display panels in the past.

[0007] To lower production cost, glass is the preferred material for forming the substrate. When a glass substrate is used, the polysilicon layer within the thin film transistors must be produced at a temperature below 500°C. A number of methods for annealing the amorphous silicon at a lower temperature have been developed. One of the most convenient and widely adopted methods is laser annealing. Laser annealing is capable of producing high quality, con-

tamination-free and low-defect-density polysilicon layer. These polysilicon thin film transistors fabricated at a relatively low annealing temperature are frequently referred to as "low temperature thin film transistors."

[0008] At present, the threshold voltage of the low temperature polysilicon thin film transistors is adjusted by performing an ion implantation or an ion shower process. However, both processes demand an ion implantation apparatus. Thus, flexibility in the manufacturing polysilicon thin film transistors is restricted.

SUMMARY OF INVENTION

[0009] Accordingly, one object of the present invention is to provide a low temperature polysilicon thin film transistor and method of manufacturing the same such that a plasma chemical vapor deposition apparatus can be selected to adjust the threshold voltage of the low temperature thin film transistor. Hence, the process for fabricating the low temperature polysilicon thin film transistor is more flexible.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of fabricating a low temperature polysilicon thin film tran-

sistor. The low temperature polysilicon thin film transistor has a channel region. One aspect of the present invention is that a plasma treatment to the channels carried out to the channel region for adjusting the threshold voltage of the low temperature polysilicon thin film transistor.

[0011] The present invention also provides a method of fabricating a low temperature polysilicon thin film transistor. First, an amorphous silicon layer is formed over a substrate. Thereafter, a plasma treatment is carried out to adjust the threshold voltage. A laser annealing process is performed to transform the amorphous silicon layer into a polysilicon layer. The polysilicon layer is next patterned to form a plurality of island polysilicon layers. A channel region is formed in each island polysilicon layer and then a doped source/drain region is formed on each side to the channel region. Finally, a gate is formed over the channel region.

[0012] According to one embodiment of the present invention, a plasma treatment is carried out using oxygen-containing plasma such as nitrous oxide (N_2O) plasma so that the threshold voltage of the thin film transistor is adjusted in the negative direction. Alternatively the plasma treatment is carried out using hydrogen-containing plasma such as

ammonia plasma (NH_3) or hydrogen plasma (H_2) so that the threshold voltage of the thin film transistor is adjusted in the positive direction. In addition, the desired shift in threshold voltage of the low temperature polysilicon thin film transistor can be set by adjusting the processing time or varying the radio frequency power in the plasma treatment.

[0013] The present invention also provides a low temperature polysilicon thin film transistor comprising a polysilicon layer, a gate and a gate insulation layer. The gate insulation layer is positioned between the gate and the polysilicon layer. The polysilicon layer has a channel region. One aspect of the present invention is that the concentration of oxygen within the channel region is between 1E19 to1E23 atoms/cc while the concentration of nitrogen within the channel region is between 5E16 to 1E19 atoms/cc.

[0014] Because the present invention uses existing equipment such as plasma chemical vapor deposition (PECVD) apparatus to carry out a plasma treatment and adjust the threshold voltage of the thin film transistor is the positive or the negative direction, there is no need to use an ion implantation apparatus. Hence, the manufacturing pro-

cess according to the present invention is more flexible.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0017] Figs. 1A to 1J are schematic cross-sectional views showing the progression of steps for fabricating a low temperature polysilicon thin film transistor according to one preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0018] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like

parts.

[0019] Figs. 1A to 1J are schematic cross-sectional views showing the progression of steps for fabricating a low temperature polysilicon thin film transistor according to one preferred embodiment of the present invention. First, as shown in Fig. 1A, a buffer layer is selectively formed over a substrate 100. The buffer layer is a stack layer comprising a silicon nitride layer 102 and silicon oxide layer 104, for example. The buffer layer mainly serves to increase the adhesive strength of the substrate 100 with a subsequently formed polysilicon layer and to prevent any metallic ions such as sodium ions in the substrate 100 from contaminating the polysilicon layer. Thereafter, an amorphous silicon layer 106 is formed over the silicon oxide layer 104.

[0020] As shown in Fig. 1B, a plasma treatment 108 is carried out to adjust the threshold voltage of the low temperature polysilicon thin film transistor. The plasma treatment 108 can be performed using existing equipment such as the plasma-enhanced chemical vapor deposition (PECVD) apparatus. For example, oxygen-containing plasma such as nitrous oxide (N_2O) plasma is used to adjust the threshold voltage of the thin film transistor in the negative direction

or hydrogen-containing plasma such as ammonia plasma (NH_3) or hydrogen plasma (H_2) is used to adjust the threshold voltage of the thin film transistor in the positive direction. In addition, the desired shift in threshold voltage of the low temperature polysilicon thin film transistor can be set by adjusting the processing time or varying the radio frequency power in the plasma treatment 108.

[0021] As shown in Fig. 1C, a laser annealing process including excimer laser annealing is performed. In Fig. 1C, the hollow white arrow representing a beam of laser sweeps across the surface of the substrate 100 along the direction 112 so that the amorphous silicon inside the amorphous silicon layer 106 is able to melt and re-crystallize into a polysilicon layer 114.

[0022] As shown in Fig. 1D, the polysilicon layer 114 is patterned to form a plurality of island polysilicon layers 114a, 114b. Since polysilicon has a relatively high electron mobility, peripheral circuits including complementary metal-oxide-semiconductor (CMOS) transistors can also be fabricated within the peripheral region outside the display region when the thin film transistor array inside the display region is fabricated. Thus, the CMOS process for fabricating P-type and N-type thin film transistors is also de-

scribed. In the following, the island polysilicon layer 114a is a portion of the desired P-type thin film transistor and the island polysilicon layer 114b is a portion of the desired N-type thin film transistor, for example. However, the simultaneous fabrication of the P-type and the N-type thin film transistors serves as an example of the fabrication process only and should not be construed as a limitation of the present invention.

[0023] As shown in Fig. 1E, a patterned photoresist layer 116 is formed over the substrate 100 to cover the island polysilicon layer 114a and a portion of the island polysilicon layer 114b and expose the upper surface on each side of the island polysilicon layer 114b. Thereafter, an n^+ doping process 118 is carried out to form the doped source/drain regions 120 of an N-type thin film transistor on each side of the island polysilicon layer 114b.

[0024] As shown in Fig. 1F, the patterned photoresist layer 116 is removed. Thereafter, a gate insulation layer 112 is formed over the island polysilicon layers 114a, 114b and the silicon oxide layer 104. Another patterned photoresist layer 124 is formed over the gate insulation layer 122 to cover the island polysilicon layer 114a and a portion of the polysilicon layer 114b and expose the area within the is-

land polysilicon layer 114b adjacent to the doped source/drain region 120. An n- doping process 126 is carried out to form lightly doped drain regions 128 in the N-type thin film transistor and simultaneously defined a channel region 130 between the lightly doped drain regions 128.

[0025] As shown in Fig. 1G, the patterned photoresist layer 124 is removed. Thereafter, another patterned photoresist layer 132 is formed over the gate insulation layer 122 to cover the island polysilicon layer 114b and a portion of the island polysilicon layer 114a and expose the upper surface on each side of the island polysilicon layer 114b. A p+ doping process 134 is carried out to form the doped source/drain regions 136 of a P-type thin film transistor and defined a channel region 138 between the doped source/drain regions 136.

[0026] As shown in Fig. 1H, the patterned photoresist layer 132 is removed. An activation process can be performed selectively before fabricating the gate. Thereafter, gates 140a, 140b are formed over the channel regions 138 and 130 respectively. An inter-layer dielectric 142 is formed over the substrate 100 to cover the island polysilicon layers 114a, 114b and the gates 140a, 140b.

[0027] As shown in Fig. 1I, a plurality of openings 144 is formed

in the inter-layer dielectric 142 and the gate insulation layer 122. The openings 144 expose the doped source/drain regions 136 and 120. Thereafter, a plurality of source/drain metallic contacts 146 are formed over the inter-layer dielectric 142 and within the openings 144 so that the source/drain metallic contacts 146 are electrically connected to the doped source/drain regions 136 and 120.

[0028] As shown in Fig. 1J, a passivation layer 148 is formed over the substrate 100. Thereafter, an opening 150 that exposes a portion of the source/drain metallic contact 146 is formed in the passivation layer 148. The passivation layer 146 is a silicon nitride layer, for example. Finally, a pixel electrode 152 is formed over the passivation layer such that the pixel electrode and the source/drain metallic contact 146 are electrically connected via the opening 150. The pixel electrode 152 is fabricated using a material including, for example, indium-tin oxide (ITO). Because existing equipment is used to carry out the plasma treatment for adjusting the threshold voltage of the polysilicon thin film transistors in the positive or the negative direction, the manufacturing process is more flexible.

[0029] In addition, as shown in Fig. 1J, the low temperature

polysilicon thin film transistor of the present invention at least comprises a pair of island polysilicon layers 114a, 114b, a pair of gates 140a, 140b and a gate insulation layer 122. The gates 140a, 140b are positioned over a substrate 100. The island polysilicon layers 114a, 114b are positioned between the gates 140a, 140b and the substrate 100. The gate insulation layer 122 is positioned between the gates 140a, 140b and the island polysilicon layers 114a, 114b. Furthermore, the island polysilicon layer 114a has a channel region 138 and a pair of doped source/drain regions 136. The channel region 138 is positioned underneath the gate 140a and the doped source/drain regions 136 are positioned on each side to the channel region 138. Similarly, the island polysilicon layer 114b has a channel region 130 and a pair of doped source/drain regions 120. The channel region 130 is positioned underneath the gate 140b and the doped source/drain regions 120 are positioned on each side to the channel region 130.

[0030] The concentration of oxygen within the channel regions 138, 130 are between 1E19 to1E23 atoms/cc while the concentration of nitrogen within the channel regions 138, 130 are between 5E16 to 1E19 atoms/cc if, for example,

nitrous oxide (N_2O) is used in the plasma treatment. In addition, the method according to the present invention can be applied to fabricate other types of thin film transistors including the bottom gate low temperature polysilicon thin film transistors as well.

[0031] One major aspect of the present invention is the utilization of existing equipment such as a plasma-enhanced chemical vapor deposition apparatus to perform a plasma treatment of the amorphous silicon layer and adjust the threshold voltage of the thin film transistors in a positive or a negative direction before laser annealing. Unlike the conventional method, using an ion implantation apparatus to perform an ion implantation operation is non-essential. Hence, the fabrication process is more flexible.

[0032] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of the present invention provided they fall within the scope of the following claims and their equivalents.